WHAT IS CLAIMED IS:

1. An electrical system configured for alternative selectable low-power operation or sampling operation during a symmetrical noise invariant time period, said electrical system comprising:

a counter for determining proximity to sampling operation; and

a switch to select between symmetrical noise invariant operation and a low-power mode of operation.

2. A system for controlling a multiplier comprising:

a multiplier;

a counter for determining proximity to sampling operation in said multiplier; and

a switch to select between symmetrical noise invariant operation and a low-power mode of operation.

3. The system according to claim 2 wherein said multiplier includes a plurality of rows each configured for selective selection and deselection to enable low power operation.

4. The system according to claim 3 comprising a switch for a selected row to enable selection and deselection of the selected row for multiplication operation.

5. The system according to claim 4 including at least a single multicell circuit connected with a selected one of the rows of the multiplier, said multicell circuit being configured to include an adder and to receive an enable signal from a preceding row.

6. The system according to claim 5 wherein each said multicell circuits is configured to, upon receipt of an enable signal, to activate its adder and generate a

done signal which in turn is adapted to activate a next adder, and to signal to a switch in a next row that the present row is finished.

7. The system according to claim 6 wherein each of said row switches is controlled by a NOOP signal on its associated bus.

8. The system according to claim 7 wherein a received signal is other than a NOOP signal, causes the receiving row to begin an addition process for that row.

9. The system according to claim 8 wherein an enable signal to a selected row is suppressed by an associated switch and an enable signal is passed to a next in order switch in a next row.

10. The system according to claim 9 wherein when an enable signal for a particular row is suppressed, the applicable row does not calculate its sums and carrys.

11. The system according to claim 10 wherein a multicell circuit passes the sums and carries from the prior row and makes it available to the next row.

12. The system according to claim 11 wherein each multicell circuit determines whether the prior row was a NOOP or a normal operative evolution.

13. The system according to claim 3, wherein each of said plurality of rows includes a plurality of blocks of computational circuitry.

14. The system according to claim 13, wherein each of said plurality of blocks of computational circuitry is

configured to provide a data valid signal to an adjacent block, to enable further processing.

15. A digital multiplier having an array of computational units arranged in rows and columns, said digital multiplier comprising:

a counter for determining proximity to sampling operation; and

a switch to select between symmetrical noise invariant operation and a low-power mode of operation.

16. A method of operating a digital multiplier having an array of computational units arranged in rows and columns, said digital multiplier comprising:

determining whether sampling operation is proximate; and

switching between a low power mode and a low noise mode of operation.

17. A digital multiplier having an array of cells, each having an enable/disable input such that each of said cells is active or inactive in response to the state of said enable/disable input, comprising;

a cell control unit which provides enable/disable inputs to at least one of said cells in response to input data to said multiplier and in response to an indication with respect to the proximity of sampling operation.

18. A switch circuit for a multiplier system, said switch circuit configured selectively to activate and deactivate selected digital circuitry during power saving and noise reduction modes of operation, said switch circuit comprising:

a switch for producing first and second output signals including respectively a row enable and a bypass out signal, said switch operating in response

to first, second, and third input signals including respectively a bypass in signal, a row done signal, and a composite NOOP and noise signal; and

a logic circuit for producing a composite NOOP and noise signal from a row NOOP signal and a noise signal.

19. The switch circuit according to claim 18, wherein said switch includes an output NOR gate to produce a row enable circuit, and a AND gate to produce a bypass out signal.

20. The switch circuit according to claim 19, wherein said switch includes first and second input NOR gates connected to and driving said output NOR gate, said first input NOR gate receiving a bypass in signal and a composite row NOOP and noise signal, and said second input NOR gate receiving a row done signal and a composite row NOOP and noise signal.

21. The switch circuit according to claim 18, wherein said switch includes an input AND gate receiving a bypass in signal and a row done signal, said input NAND gate driving said output AND gate.

22. The switch circuit according to claim 21, wherein said input AND gate receives a composite row NOOP and noise input signal.

23. The switch circuit according to claim 18, wherein said output AND gate receives a bypass in signal and a row done signal.

24. The switch circuit according to claim 18, wherein said logic circuit is a AND gate receiving row NOOP and noise control signals.

25. A method of operating a digital multiplier in successive row addition in connection with an analog system performing analog sampling operations subject to completion of predetermined digital clock cycles, comprising:

selectively skipping a row addition operation to enable power saving when a row NOOP condition is identified;

overriding the selective skippage of row additions in the proximity of analog sampling operation; and

resuming selective row skippage upon departure from the proximity of analog sampling operation.